CLAIMS

What is claimed is:

1. A filter, comprising:

a tap multiplication circuit;

a tap digital-to-analog ("DAC") unit coupled to the tap multiplication circuit; and

a plurality of clocks that control timing associated with the tap multiplication circuit and that permit one tap multiplication to be output while another tap multiplication is being computed;

wherein said tap multiplication circuit comprises a plurality of tap multiplication units, each tap multiplication unit comprising a first transistor that is controlled to output a tap coefficient current, and a second transistor that is controlled to provide current through a conducting branch that is separate from a branch in which the tap coefficient current is output, wherein the first transistor and the second transistor are not on at the same time.

2. The filter of claim 1 wherein the tap DAC unit comprises a break-before-make switch that, when a coefficient bit transitions logic states, precludes a gate of a current source from being grounded and then couples the gate to a control voltage.

3. The filter of claim 1 further comprising a replica bias circuit coupled to the tap multiplication circuit and the DAC unit, the replica bias circuit provides substantially constant DAC steps regardless of variations in voltage associated with a current source in the tap DAC unit.

4. A filter, comprising:

a tap multiplication circuit;

a tap digital-to-analog ("DAC") unit coupled to the tap multiplication circuit;

means for controlling timing associated with the tap multiplication circuit and for permitting one tap coefficient to be output while another tap coefficient is being computed; and

means for precluding a gate of a current source from being grounded and then for coupling the gate to a control voltage.

5. The filter of claim 4 further comprising means for providing substantially constant DAC steps regardless of variations in voltage associated with a current source in the tap DAC unit.

6. A communication apparatus, comprising:

a summer;

a slicer coupled the summer and that generates sample decisions; and

a filter coupled to the slice and the summer that receives equalization coefficients and sample decisions and generates and provides an equalization signal to the summer, the filter comprising a tap multiplication circuit, a tap digital-to-analog ("DAC") unit coupled to the tap multiplication circuit, and a plurality of clocks that control timing associated with the tap multiplication circuit and

that permit one tap coefficient to be output while another tap coefficient is being computed.

wherein said tap multiplication circuit in the filter comprises a plurality of tap multiplication units, each tap multiplication unit comprising a first transistor that is controlled to output a tap coefficient current, and a second transistor that is controlled to provide current through a conducting branch that is separate from a branch in which the tap coefficient current is output, wherein the first transistor and the second transistor are not on at the same time.

7. The apparatus of claim 6 wherein the tap DAC unit comprises a break-before-make switch that, when a coefficient bit transitions logic states, precludes a gate of a current source from being grounded and then couples the gate to a control voltage.

8. The apparatus of claim 6 further comprising a replica bias circuit coupled to the tap multiplication circuit and the DAC unit, the replica bias circuit provides substantially constant DAC steps regardless of variations in voltage associated with a current source in the tap DAC unit.

9. A method, comprising:

generating currents associated with tap coefficients

controlling sample decisions based on the currents; and

permitting current associated with one tap coefficient to be output while pre-computing current associated with at least one other tap coefficient.

10. The method of claim 9 further comprising replicating a current source control voltage to maintain substantially constant digital-to-analog conversion steps.

11. The method of claim 9 further comprising breaking a grounded gate voltage associated with a transistor that generates said currents and then establishing a gate voltage at a control voltage level.